| L Number | Hits | Search Text | DB | Time stamp |
|---|---|---|---|---|
| - | 2729924 | s horizontal source line | USPAT; US-PGPUB; IBM TDB | 2001/11/15 11:38 |
| - | 145624 | (s horizontal source line) and isolation | USPAT; US-PGPUB; IBM TDB | 2001/11/15 11:39 |
| - | 2635886 | s "12" and vertical source line | USPAT; US-PGPUB; IBM TDB | 2001/11/15 11:43 |

L7 ANSWER 5 OF 26 USPATFULL

TI Scalable flash **EEPROM** memory cell, method of manufacturing and operation thereof

AB A scalable flash **EEPROM** cell has a semiconductor substrate with a drain and a source and a channel therebetween. A select gate is positioned. . .

SUMM The present invention relates to an electrically erasable and programmable read-only non-volatile memory (**EEPROM**) cell or, more specifically, a flash **EEPROM**.

SUMM One prior art flash memory device is a stack gate flash **EEPROM** where a single stack-gate transistor constitutes the memory cell. It programs as a traditional UV-erasable EPROM, using the mechanism of. . .

DETD . . . 16 respectively, by ion implantation of a second conductor type, such as arsenic. Typically, spacers are placed adjacent to the **floating gate** 24 and the select gate 20. The arsenic is implanted at a concentration of approximately 1.times.10.sup.15 to 1.times.10.sup.16 ions/cm.sup.2, and. . . required to form the LDD junction of the periphery transistors for reducing hot electron effects of short channel transistors, the **implanted arsenic** will have little or no overlap with the **floating gate** 24. Thereafter, lateral diffusion of the arsenic implant will bring the arsenic dopant to a region substantially near the side wall of the **floating gate** 24 and select gate 20. However, the overlap between the **floating gate** 24 and the source region 14 is not sufficient to permit Fowler-Nordheim tunnelling of a magnitude required for the operation. . . a second implant is required to form a deeper source region 14 which overlaps to a greater degree with the **floating gate** 24;

DETD From the foregoing it can be seen that the present flash **EEPROM** memory cell and array can be operated with very low programming current so that it can be supported by an. . .

PI US 6057575 20000502

L7 ANSWER 6 OF 26 USPATFULL

SUMM . . . for further background information on Fowler-Nordheim tunneling, hot electron injection, and flash memory structures: U.S. Pat. No. 5,077,691 entitled "Flash **EEPROM** Array With Negative Gate Voltage Erase Operation; U.S. Pat. No. 4,698,787 entitled "Single Transistor Electrically Programmable Memory Device And Method;. . .

DETD P- island 208 is floating in some embodiments and is grounded in other embodiments. Electrons tunnel from the **floating gate** 202 to the drain region 204. In some embodiments, the structure of FIG. 39 is fabricated in accordance with the. . . step of removing the remaining thick oxide (between FIGS. 18 and 19). The N+ buried layer 201 is formed by **implanting arsenic** or phosphorous with an implant energy in a range of approximately 400-800 KeV and a preferred implant energy of approximately. . .

PI US 6043122 20000328

=> d pn, kwic l2 1-3

L2 ANSWER 1 OF 3 USPATFULL
PI US 6072212 20000606
SUMM . . . in U.S. Pat. No. 5,019,527. In prior-art Flash EPROMs of the type described in exemplary U.S. Pat. No. 5,019,527, a **horizontal source line** connects to the sources of each memory cell in a row of an array of such memory cells. The term. . .

L2 ANSWER 2 OF 3 USPATFULL
PI US 5858839 19990112
SUMM . . . in U.S. Pat. No. 5,019,527. In prior-art Flash EPROMs of the type described in exemplary U.S. Pat. No. 5,019,527, a **horizontal source line** connects to the sources of each memory cell in a row of an array of such memory cells. The term. . .

L2 ANSWER 3 OF 3 USPATFULL
PI US 5659500 19970819
SUMM . . . a manner that allows more room for the contact structure, including insulator space and including masking tolerances, to the diffused **horizontal source line**. The bend in the stacks results in a need for an area with a relatively large horizontal distance for formation. . .
DETD FIG. 6 is a simulated cross-sectional view of a field-effect structure having symmetrical source-type diffusions that represent the **horizontal source line** 17 diffusions and the vertical source line 17a diffusions of this invention on either side of the straight stack ST,. . .

=> d pn, kwic 1-4

L4 ANSWER 1 OF 4 USPATFULL
PI US 6243293 B1 20010605
AB . . . and drain regions, a floating gate extending over a portion of the channel with a first dielectric layer therebetween, a **control gate** extending over a portion of the floating gate through a second dielectric layer, and a program gate extending above the. . . the drain voltage to the floating gate, thereby establishing a high voltage at a point in the channel between the **control gate** and the floating gate and ensuring a high hot-electron injection towards the floating gate.
SUMM . . . gate overlies the whole channel area from above the source region to above the drain region, and a single external **control gate** is arranged on top of the floating gate. After floating gate formation, a high quality dielectric layer (usually oxide-nitrideoxide (ONO)). . .
SUMM . . . portion of the channel, (iii) a second silicon dioxide insulating layer formed over the floating gate, and (iv) a polysilicon **control gate** formed over the second insulating layer above the floating gate and having an access portion that extends above the remaining. . .
SUMM . . . a channel region and a drain region formed therein. The HIMOS.TM. cell has three separate gates. These gates are the **control gate** (CG), the floating gate (FG), and the program gate (PG).
SUMM The **control gate** CG and program gate PG are formed in a second polysilicon layer. The **control gate** overlies the floating gate and further extends to overlie a second portion of the channel uncovered by the floating gate. As described in the priority applications, the **control gate** is insulated from the floating gate and from the second portion of the channel by an interpoly oxide layer.
SUMM . . . floating gate, extends over the uncovered portion of the channel and is covered later in the fabrication process by the **control gate**.
SUMM . . . oxide layer between the channel and the floating gate, and a second oxide layer between the floating gate and the **control gate**. As is common in stacked-gate devices, this second oxide layer may be an ONO layer. In turn, as is also. . . devices, this second oxide layer of Bergemont is present only on top of the floating gate and not under the **control gate** on the uncovered portion of the channel region.
SUMM . . . the polysilicon and oxide layers. In this way, the first oxide layer would remain over the channel region under the **control gate** that is deposited thereafter, unlike in the HIMOS.TM. cell.
SUMM . . . arise in forming the equivalent of a dielectric layer between the adjacent vertical sidewalls of the floating gate and the **control gate** access portion. As a result, the interpoly leakage of the device could be limited by the (polyoxide) sidewall of the. . .
SUMM In forming the HIMOS.TM. cell, in contrast, the interpoly oxide growth is advantageously combined with the oxide under the **control gate**. By combining these steps, the processing cost is considerably reduced. At the same time, however, the resulting HIMOS.TM. cell is. . .
DRWD . . . a HIMOS.TM. symbol for an array description, including

terminals for the a source junction (S), a drain junction (D), a **control gate** (CG) and a program gate (PG);

DETD . . . each column of cells has a separate bitline. The floating gates are formed in the first polysilicon layer, while the **control gate** and the program gate are formed in the second polysilicon layer. Each program gate serves as a coupling capacitor for. . .

DETD The **control gate** forms the wordline of the array and is running horizontally over the active transistor area and over the source and. . . same row. The shape of the wordline has been designed in order to minimize the parasitic coupling coefficient between the **control gate** and the floating gate. On the other hand, the program gates of two adjacent wordlines are merged into one program.

. .

DETD . . . For instance, a 0.7 .mu.m version of such a cell provides about 120 .mu.A of current for a 3 V **control-gate** voltage. In a 64 kbit product, however, this is reduced to only 70 .mu.A for an average cell. Salicidation will. . .

DETD . . . arise that compromise scalability. One requirement, for example, is that the part of the channel that is controlled by the **control gate** will have to be drawn at about 1 .mu.m in order to obtain a final channel length (after processing) of. . .

DETD . . . at the source side of the cell. As a result, the part of the channel that is controlled by the **control gate** can be limited to the minimum feature size. Thus, for instance, where the bitline is shared between adjacent columns (the. . .

DETD . . . potential, which ensures a high read-out speed, even in large memory arrays. Another advantage is the straightforward decoder design: the **control gate** forms the wordline, each column of cells connects to a separate bitline, and source decoding becomes redundant. The main disadvantage,. . .

DETD . . . 45.degree.). This implies that the WL is bent around these source contacts, which also minimizes the parasitic coupling ratio between **control gate** and floating gates. The coupling ratio, in one embodiment, is at least 30%. The bitline contact is then placed in. . .

CLM What is claimed is:

. . . and drain regions; a floating gate extending over a portion of the channel with a first dielectric layer therebetween; a **control gate** extending over a portion of said floating gate through a second dielectric layer; a common polysilicon wordline interconnecting said control. . . said drain voltage to said floating gate, thereby establishing a high voltage at a point in said channel between said **control gate** and said floating gate and ensuring a high hot-electron injection towards said floating gate.

2. The matrix as claimed in claim 1 wherein said **control gate** is extending from above said source region over another portion of the channel through said second dielectric layer.

. . . claim 1 wherein the floating gate of each of said EEPROM cells includes a first portion extending from below said **control gate** to below said program gate.

. . . from said channel, the program gate capacitively coupled through the

dielectric layer to said second floating gate portion, and the **control gate** laterally remote in a second direction from said program gate and extending through the dielectric oxide layer over said first. . .

. . . contact shared between adjacent cells; a common bit line contact shared between adjacent cells; a common polysilicon program line; a **vertical source line** interconnecting the common source line contacts of cells along adjacent columns; and a common vertical bit line interconnecting the common. . .

L4 ANSWER 2 OF 4 USPATFULL

PI US 6072212 20000606

AB . . . conductivity-type forms the channel of at least one memory cell (10) in the array. A floating gate (13) and a **control gate** (14) of that memory cell (10) are located over, and insulated from, a junction of the first diffusion and the. . .

SUMM . . . that all of the sources of the memory cells in an array are connected to a common electrode. Each metal **vertical source line** typically requires a space equivalent to about one and one-half columns of memory cells. The vertical source lines are placed. . .

SUMM . . . second diffusion of first conductivity-type forms the channels of the memory cells in that subarray. A floating gate and a **control gate** of that memory cell are located over, and insulated from, a junction of the first diffusion and the second diffusion.. . .

DETD . . . invention. Each cell is a floating-gate transistor 10 having a source 11, a drain 12, a floating gate 13, a **control gate** 14. Each of the control gates 14 in a row of cells 10 is connected to a horizontal wordline 15,. . .

DETD . . . (or microprocessor 21) to place a gate voltage Vg of about +10V on a selected wordline 15, including a selected **control-gate** 14. Optionally, Read/Write/Erase control circuit 21, (or microprocessor 21) may place a negative voltage of about -1V or -2V on. . . (with Vg at 0V). For memory cells 10 fabricated in accordance with the example embodiment, the coupling coefficient between a **control gate** 14/wordline 15 and a floating gate 13 is approximately 0.6. Therefore, a programming gate voltage Vg of 10V, for example, on a selected wordline 15, including the selected **control gate** 14, places a voltage of approximately +6V on the selected floating gate 13. The voltage difference between the floating gate. . . the source-drain path under the floating gate 13 of the selected cell 10 non-conductive with a positive read voltage on **control gate** 14, a state that is optionally read as a "zero" bit. Deselected cells 10 have source-drain paths under the floating. . .

CLM What is claimed is:

. . . one said third diffused region in said substrate located at one edge of a said floating gate and a said **control gate**, said third diffused region isolated in said second diffusion to form the drain of a said memory cell.

L4 ANSWER 3 OF 4 USPATFULL

PI US 5858839 19990112
AB . . . conductivity-type forms the channel of at least one memory cell
(10) in the array. A floating gate (13) and a **control gate** (14) of that memory cell (10) are located over, and insulated from, a junction of the first diffusion and the. . .
SUMM . . . that all of the sources of the memory cells in an array are connected to a common electrode. Each metal **vertical source line** typically requires a space equivalent to about one and one-half columns of memory cells. The vertical source lines are placed. . .
SUMM . . . second diffusion of first conductivity-type forms the channels of the memory cells in that subarray. A floating gate and a **control gate** of that memory cell are located over, and insulated from, a junction of the first diffusion and the second diffusion.. . .
DETD . . . invention. Each cell is a floating-gate transistor 10 having a source 11, a drain 12, a floating gate 13, a **control gate** 14. Each of the control gates 14 in a row of cells 10 is connected to a horizontal wordline 15,. . .
DETD . . . (or microprocessor 21) to place a gate voltage Vg of about +10V
on a selected wordline 15, including a selected **control-gate** 14. Optionally, Read/Write/Erase control circuit 21, (or microprocessor 21) may place a negative voltage of about -1V or -2V on. . . (with Vg at 0V). For memory cells 10 fabricated in accordance with
the example embodiment, the coupling coefficient between a **control gate** 14/wordline 15 and a floating gate 13 is approximately 0.6. Therefore, a programming gate voltage Vg of 10V, for example, on a selected wordline 15, including the selected **control gate** 14, places a voltage of approximately +6V on the selected floating gate 13. The voltage difference between the floating gate. . . the source-drain path under the floating gate 13 of the selected cell 10 non-conductive with a positive read voltage on **control gate** 14, a state that is optionally read as a "zero" bit. Deselected cells 10 have source-drain paths under the floating. . .
CLM What is claimed is:
. . . diffused region including the channel of at least one memory cell in said array; forming a floating gate and a **control gate** of said at least one memory cell over, and insulated from, a junction of
said first diffused region and said. . . least one third diffused region of said second conductivity-type, said third diffused region formed using said floating gate and said **control gate** as a mask, said third diffused region isolated in said second diffusion to form the drain of said at least. . .

L4 ANSWER 4 OF 4 USPATFULL
PI US 5659500 19970819
SUMM . . . bend in the stacks results in a need for an area with a relatively large horizontal distance for formation the **vertical source line**. That distance is greater than the horizontal distance needed for each column of cells. As a result, the horizontal spacing. . . In some cases, the distortion is sufficient that dummy columns of cells are used on each side of the metal **vertical source line**, resulting in an even

greater area of non-functional structure on the chip.

SUMM These source contacts, and the metal **vertical source line** connected to those contacts, are needed because the regions under the stack are non-conductive.

DRWD FIG. 5 is a cross-section of the stack connection of this invention indicating the joined **vertical source line** diffusions of the device of FIG. 4, the cross-section designated by line B--B' of FIG. 4;

DRWD FIG. 7 is an I-V.sub.G measurement plot for the stack configuration of FIG. 6 as the **control gate** voltage V.sub.G is varied;

DETD . . . invention. Each cell is a floating-gate transistor 10 having a source 11, a drain 12, a floating gate 13, a **control gate** 14. Each of the control gates 14 in a row of cells 10 is connected to a wordline 15, and. . .

DETD . . . 21) to place a preselected first programming voltage V.sub.P1 (approx. +12 V) on a selected wordline 15, including a selected **control-gate** 14. Column decoder 19 also functions to place a second programming voltage V.sub.P2 (approx. +5 to +10 V) on a. . . V.sub.P1 at 0 V). For memory cells 10 fabricated in accordance with the example embodiment, the coupling coefficient between a **control gate** 14/wordline 15 and a floating gate 13 is approximately 0.6. Therefore, a programming voltage V.sub.P1 of 12 V, for example, on a selected wordline 15, including the selected **control gate** 14, places a voltage of approximately +7.2 V on the selected floating gate 13. The voltage difference between the floating. . . the source-drain path under the floating gate 13 of the selected cell 10 nonconductive with a positive read voltage on **control gate** 14, a state which is read as a "zero" bit. Deselected cells 10 have source-drain paths under the floating gate. . .

DETD . . . cells 10. As a result, the spacing between field oxide regions FO is non-uniform, the spacing being greater at the **vertical source line** 17a. Because the spacing between field oxide regions FO is non-uniform, the field oxide regions FO adjacent the vertical source. . .

DETD . . . 13 is formed from a layer of doped polysilicon insulated from the channel 24 by gate insulator 25. The polysilicon **control gate** 14, which is a part of the wordline 15 of FIG. 1, is insulated from the floating gate 13 by. . .

DETD . . . cross-section at line B--B' of FIG. 4. FIG. 5 shows diffusions under stack ST to form the diffused part of **vertical source line** 17a. The diffused part of **vertical source line** 17a is formed by implanting phosphorous on both sides of each stacked layer ST at the same time the sources. . . resistance of the combined vertical source conductor 17a. FIG. 4 also illustrates a narrower width of space required by the **vertical source line** 17a of this invention as compared to the width of space required by the prior-art **vertical source line** 17a of FIG. 2. The width of space required by the **vertical source line** of FIG. 4 is identical to the width of space required by one column of cells 10. In effect, there. . . oxide regions FO. And any need for the two vertical "dummy" columns of cells 10 on either side of a **vertical source line** 17a is eliminated,

along with the space required for those two dummy columns of cells 10.

DETD . . . cross-sectional view of a field-effect structure having symmetrical source-type diffusions that represent the horizontal source line 17 diffusions and the **vertical source line** 17a diffusions of this invention on either side of the straight stack ST, respectively. In FIG. 6, lines DR represent. . .

DETD As mentioned previously and as illustrated in FIG. 11, the proposed straight stack ST layout over the **vertical source line** 17a may optionally be trimmed by 0.1 to 0.2 cm from the nominal stack S.sub.T line width. This results in. . .

=> d his

(FILE 'HOME' ENTERED AT 11:46:23 ON 15 NOV 2001)

FILE 'USPATFULL' ENTERED AT 11:46:34 ON 15 NOV 2001

L1 3 S CONTROL GATE AND HORIZONTAL SOURCE LINE
L2 3 S HORIZONTAL SOURCE LINE
L3 13 S VERTICAL SOURCE LINE
L4 4 S L3 AND CONTROL GATE